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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/919,361	07/30/2001	Steven C. Woo	RB1-026US	2536

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EXAMINER

VERBRUGGE, KEVIN

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 12/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/919,361

Applicant(s)

WOO ET AL.

Examiner

Kevin Verbrugge

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 November 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26,28-35,38-40,52 and 53 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26,28-35,38-40,52 and 53 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

This final Office action is in response to Amendment B, paper #8, filed 11/18/03 by fax which canceled claim 27. Claims 1-26, 28-35, 38-40, 52, and 53 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-8, 10, 11, 12, 14-18, 26, 28, 29, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Regarding claims 1, 4, 5, 11, 14, 15, 16, and 26, Ohsawa discloses the claimed plurality of dynamically refreshable memory cells as the DRAM cell array in Figs. 4 and 5.

He shows the claimed dynamically changeable use registers corresponding to groups of memory cells as refresh flags, shown in Figs. 4 and 5.

His memory device is configured to omit refreshing of memory cells that are not in use, as claimed, as indicated by the refresh flags.

Regarding claims 2 and 12, in section 4.3, last paragraph, Ohsawa mentions static mode which is the claimed self-refresh mode.

Regarding claims 6, 17, and 28, Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

Regarding claim 7, Ohsawa's row of memory cells is a set of memory cells.

Regarding claims 8, 18, and 29, Ohsawa's refresh flags refer to rows as claimed.

Regarding claim 10, a page of memory cells is the same as a row of memory cells.

Regarding claim 31, Ohsawa shows his use registers in the memory devices in Figs. 4, 5, 7, and 8.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, 8, 10-16, 18-20, 23-26, 29, 31-33, 35, 38-39, 52, and 53 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,167,484 to Boyer et al., hereinafter simply Boyer.

Boyer discloses a method and apparatus for leveraging history bits to optimize memory refresh performance.

Boyer discloses or suggests all of the claimed features throughout his disclosure. Particularly relevant portions of his disclosure include Figs. 2, 3, 8, 9, and 16 and passages at column 2, lines 49-60, column 3, lines 22-27, column 4, lines 14-21 and 60-64, column 5, lines 17-20, column 7, lines 12-18 and 46-51, column 8, lines 1-3 and 26-30, column 10, lines 62-67, column 14, lines 16-19 and 31-34, column 23, lines 2-7, and column 25, line 50 through column 26, line 25.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

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invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6, 9, 17, 21, 22, 28, 30, 34, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,167,484 to Boyer et al., hereinafter simply Boyer in view of "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa.

Regarding claims 6, 17, 21, 28, 34, and 40, Boyer does not mention caching in his disclosure.

Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include caching in Boyer's device to speed up system operation and it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Ohsawa's technique of not refreshing those rows that were cached to further speed up system operations by not having to refresh those rows that were cached, as taught by Ohsawa.

Regarding claim 9, Boyer's refresh flags refer to rows. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use refresh flags for a bank since this would allow an entire bank to be shutdown if its refresh flag were not set, avoiding the need to read the refresh flag of each row.

Regarding claims 22 and 30, Boyer shows that his use registers are outside the DRAM controller (Fig. 8, for example). However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to move the use registers to the memory controller to have more centralized control over the memory cells. Putting the use registers in the memory controller would speed up access to them.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 9, 13, 19, 21-25, 30, 32-35, 38-40, 52, and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al., hereinafter simply Ohsawa in view of U.S. Patent 6,167,484 to Boyer et al., hereinafter simply Boyer.

Regarding claims 3, 13, 19, 25, 32, 33, 35, 38, 39, 52, and 53, Ohsawa does not disclose the claimed recent access flags or keeping track of which memory cells have been accessed in a manner that refreshed the memory cells in a previous memory cycle.

Boyer discloses the recent access flags and keeping track of which memory cells have been accessed in a manner that refreshed the memory cells in a previous memory cycle (by being read or written).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Boyer's recent access flags in Ohsawa's device to further reduce the number of refresh cycles required to maintain data because Boyer's device is directed to the same goal of reducing the number of refreshes required, thereby reducing power consumption and enhancing processing speed by improving bandwidth.

Regarding claims 21, 34, and 40, Ohsawa mentions the claimed caching of memory rows and not refreshing those rows at section 3.2.

Regarding claims 23, Ohsawa shows his use registers in the memory devices in Figs. 4, 5, 7, and 8.

Regarding claim 24, Ohsawa's refresh flags refer to rows as claimed.

Regarding claim 9, Ohsawa's refresh flags refer to rows. However, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use refresh flags for a bank since this would allow an entire bank to be shutdown if its refresh flag were not set, avoiding the need to read the refresh flag of each row.

Regarding claims 22 and 30, Ohsawa shows that his use registers are in the memory devices, however, It would have been obvious to one of ordinary skill in the art at the time the invention was made to move the use registers to the memory controller to have more centralized control over the memory cells. Putting the use registers in the memory controller would speed up access to them.

Response to Arguments

Claims similarly argued are addressed only regarding the first claim mentioned, but the remarks below apply to all claims similarly argued.

On page 13, first paragraph, Applicant states that the amendments to the claims have been made in an effort to impart precision to the claims by more particularly pointing out the invention, rather than to avoid prior art. Indeed, the Examiner has determined that the amended claims still do not avoid the cited prior art and so the previous rejections are maintained and made final herein.

Claim 1

Regarding claim 1, on page 14, first paragraph, Applicant argues that the new limitation "the use registers are implemented adjacent to the memory cells" is not taught or suggested by any of the prior art of record.

In paragraph 3 of page 14, Applicant's representative asserts that "after reviewing the identified sections [of Boyer] he is unsure how these sections relate to the

claimed combination of features such as set forth in claim 1.” Further, Applicant’s representative argues that “Boyer at a minimum fails to teach, disclose, or suggest any ‘use registers’ or that the use registers being [sic] ‘implemented adjacent to the memory cells’ (see, e.g., Fig. 2 of Boyer)” (page 15, first paragraph).

In response, first of all, it is noted that in Boyer’s discussion of Fig. 2 he teaches that unused memory locations “may be flagged as unused so that unused memory is not needlessly refreshed” (column 7, lines 50-51). This is part of one of the passages cited by the Examiner in the previous Office action and clearly teaches that Boyer anticipates use registers which indicate whether memory is in use or not in use.

An additional passage that was cited by the Examiner that directly relates to the claimed features in claim 1 is column 25, line 50 through column 26, line 25. In this passage he refers to a “valid bit” as indicating whether a particular row is in use or not and at column 26, lines 22-25, he explicitly teaches that “It would be understood by one skilled in the art that separate register bits could be used to store the valid information”, clearly anticipating the claimed use registers which indicate whether a row is in use or not.

In response to the newly claimed limitation that the use registers must be adjacent to the memory cells it is acknowledged that although perhaps Boyer is not explicit in showing that his use registers are implemented adjacent to the memory cells, he shows in Fig. 2 a history qualifier block 204 which “stores history bits 302 which keep track of the ‘freshness’ of each memory row” (emphasis added, column 7, lines 45-46, also previously cited to Applicant). This history qualifier block 204 is shown adjacent to

the DRAM tile memory array in Fig. 2 and it is clear from the passage just cited that there is a history bit or bits for each memory row being monitored. From Fig. 2 these bits are apparently adjacent to the memory array and Boyer's suggested use registers would similarly be placed adjacent to the memory rows.

Furthermore, whether Boyer actually shows the use registers or history bits physically adjacent to the memory rows is secondary in importance. Of primary importance is the fact that Boyer teaches that each row has an associated history bit and use register and this one-to-one logical relationship or association is what is crucial to his invention: each memory row is independently monitored for individual control of refresh operations. If a row is flagged as not in use, it is not refreshed at all. Similarly, if a row's history bit indicates that it was recently accessed (and therefore recently refreshed since accessing requires a refresh in addition to the read or write), then it will not be refreshed in the next refresh cycle. Both of these monitoring operations reduce the number of refresh operations required by the device and therefore save power and improve processing speed and power.

Regarding Ohsawa, at page 15, last paragraph, Applicant argues that Ohsawa's Fig. 4 is a mere illustration of correspondence between use registers and memory rows as opposed to a structural diagram. This is contradicted, however, by the caption on Fig. 4 as "An implementation of SRA" (Selective Refresh Architecture) and by the first sentence of the fourth paragraph of section 3.1 where Ohsawa teaches that Fig. 5 "shows the SRA architecture in detail". Fig. 4 shows the SRA architecture, while Fig. 5 shows the same SRA architecture but with more detail. This is clear because of the

captions on the figures and because all of the elements of Fig. 4 (refresh flags and memory rows in the cell array) are shown in Fig. 5 as well. Applicant admits as much, at page 16, first paragraph where he states that "Ohsawa clearly intended Fig. 4 not to be anything more than a simplification of Fig. 5.

In any case, the bottom line is that Ohsawa clearly shows the claimed plurality of dynamically refreshable memory cells as the DRAM cell array in Figs. 4 and 5, he shows the claimed dynamically changeable use registers as refresh flags in Figs. 4 and 5, he shows the refresh flags adjacent to the memory cells, and his memory device is configured to omit refreshing of memory cells that are not in use as indicated by the refresh flags.

Applicant has added the limitation "wherein the use registers are implemented adjacent to the memory cells" for the purpose of "more particularly pointing out the invention, rather than to avoid prior art" (page 13, first paragraph). Accordingly, it is noted that the added limitation does not avoid the prior art since Ohsawa clearly shows his refresh flags adjacent to the memory cells.

It is illustrative to note that the Applicant's own disclosure shows that this newly added limitation of use registers adjacent to memory cells does not avoid the prior art. For example, Fig. 2 shows use registers 24 adjacent to the memory rows just as in Ohsawa's Fig. 4, and at page 6, lines 18-21, Applicant teaches that "use registers 24 ... are associated respectively with individual memory cell rows" and "each bit or flag is set to indicate whether the corresponding row is actually in use" just as Ohsawa teaches.

Claim 2

Regarding claim 2, Applicant's arguments are not persuasive. Items (1) and (2) of section 3.1 are referring to determining when to stop refreshing altogether when data is no longer needed. Once data is no longer refreshed, the data is lost because it gradually "leaks out" of DRAM cells. This discussion in Ohsawa is related to when to indicate that particular rows are no longer needed and therefore can be discarded. Self-refresh, on the other hand, is a state of a DRAM device where refresh is continued, preserving the data, but power is saved because writes and reads are not permitted. Ohsawa's static mode is the same as self refresh mode, and a device performing self refresh necessarily contains the claimed self-refresh logic.

Claim 25

Regarding claim 25, the limitation of the use registers being adjacent to the memory cells is addressed in the remarks above. The recent-access flags limitation is briefly mentioned above but is elaborated here. While Ohsawa clearly shows use registers adjacent to the memory cells, he does not show recent access flags. Boyer, however, clearly shows recent access flags as history bits as discussed above in the grounds of rejection. In the discussion above it is pointed out that the history bits are shown adjacent to the memory rows in Fig. 2 of Boyer and he discusses how each row has its own bit or bits to indicate whether the corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval (see column 5, lines 17-20, column 7, lines 12-18 and 46-48, column 8, lines 26-30, and column 14, lines 16-19 and 31-34). Boyer's explicitly stated intent of

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monitoring the recent accesses is to avoid refreshing rows that were just refreshed as a result of some access. This saves power and improves operation speed.

Conclusion

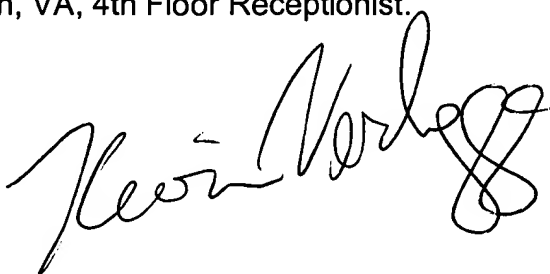
THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (703) 308-6663.

Any response to this action should be labeled appropriately (serial number, Art Unit 2188, and After-Final, Official, or Draft) and mailed to Commissioner for Patents, Washington, D.C. 20231, faxed to (703) 872-9306, or delivered to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor Receptionist.

Kevin Verbrugge
Primary Examiner
12/23/03

A handwritten signature in black ink, appearing to read "Kevin Verbrugge", with a stylized, looping flourish at the end.